Vitesse Re-Skilling Canada Inc.

Carleton University
&
Canadian Microelectronics Corporation

Present 2-week Leading-edge Training program on:

Digital Integrated Circuits Design

July 28 - August 8, 2003

Objectives:

This 2-week customized intensive training program has been designed to meet the specific needs of the semiconductor industry. It will help the participants acquire critical skills in state-of-the-art methodologies for Verilog-based FPGA specifications, design, synthesis, verification, test and layout of complex digital systems. This course will feature a combination of background materials and practical laboratory session. It is expected, upon completion of this course, participants will be ready to work in the microelectronics industry.

Instructor:

Prof. Maithem Shams:

Dr. Shams is a professor of Electronics at Carleton University. He obtained his master's and PhD degrees from the University of Waterloo. He has been in the field of VLSI for over 10 years and has published in reputable international journals and conference proceedings. He has a broad research interest, covering Design, Analysis, Modeling, Synthesis, and Testing of High-Speed and Low-Power ICs. At Carleton, he teaches VLSI courses both at the graduate and under-graduate levels. He and Dr. Knight have organized the Carleton ASIC Research Group and supervise the master and PhD students in that group.

Prof. John Knight:

Professor Knight has taught digital circuit courses at Carleton for over 20 years, all the way from the first switching-circuit course to graduate courses in ASIC synthesis, design and testing. John has also taught digital design and testing at Nortel, and was the main digital teacher for the recent Carleton-SMC Bridge Camps (similar to this course). At Carleton, he has won several awards for his teaching. His students know him for metaphors like "blaspheming the clock."

He has done extensive consulting for Mitel, Nortel and SigPro Wireless. His research has centered on low-power circuitry and behavioral synthesis.Prof. John Knight & prof. Maithem Shams of Carleton University will be delivering the course materials. Both of them teach digital design and testing courses at Carleton University and are well known nationally and internationally for their research works in Digital IC Design.

Intended Audience:

Electrical/electronic engineering graduates or equivalent, who are looking for a great career opportunity in microelectronics design industry, New hires and retrainee designers and their managers, as well as manufacturing, application and test engineers can all benefit from becoming quickly familiar with digital system design including obtaining hands-on experience on how to build realistic digital systems that will be on actual logic devices.

Benefits

This course will enable you to

- ☐ Use and acquire proficiency in Cadence, Synopsis and other design tools
- ☐ Prepare yourself for designing with hardware design languages in any environment
- ☐ Develop hands-on experience in designing with commercial programmable logic devices
- ☐ Understand comprehensively the entire chip making process
- ☐ Have a Certificate of attestation upon completion
- ☐ Stay current with the latest tools and techniques used by the Industry

Course Content

Digital IC Design Flow	CMOS Technology
Verilog HDL	Digital Building Blocks
Synthesis	Timing & System Clock
Testing & Testability	Simulation & Verification
High-Speed & Low Power VLSI Techniques	Site Visit & Wrap up

Course Fee

The fee for this short course is $4000.00 (tax included). This will include tuition, course notes, daily lunches and coffee breaks. 10% discount for 3 or more participants from the same organization.

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Venue

Room 4125, Department of Electronics, Carleton University

Registration fees and deadlines for the Training program

Completed registration form, with payment or purchase order should be received on or before Friday, July 11, 2003
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Cancellation policy for the training program

Written cancellation will be accepted if received on or before Friday, July 11, 2003. After July 11, 2003, full fees will be invoiced. Substitution is permitted at anytime at no extra charge. If there is insufficient attendance to conduct the training program, notice will be given to registrants on Monday, July 14, 2003.

How to Register

Complete and return the registration form to:

Vitesse Re-skilling Canada Inc,
1200 Montreal Rd.
Bldg. M-50
Ottawa, ON K1A 0R6

Check should be made payable to Vitesse Re-skilling Canada Inc

***** Course Capacity is limited
Register now to ensure your participation********